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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,965	02/09/2004	Afshin Momtaz	BU3368	8766

7590 09/20/2007

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EXAMINER	
DEPPE, BETSY LEE	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
09/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,965	MOMTAZ, AFSHIN	
	Examiner	Art Unit	
	Betsy L. Deppe	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 17-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 17-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2007 and 09 February 2004* is/are: a)☒ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed July 27, 2007 have been fully considered but they are not persuasive.

2. In response to applicant's arguments that the drawings and specification show the recited frequency acquisition loop (see pages 11 and 12), the Examiner respectfully disagrees with the applicant. The applicant points out that Figure 5 shows a frequency acquisition loop that maintains a "frequency between an extracted clock signal and a binary signal." Based on the Examiner's understanding of the description on page 8, line 8 - page 9, line 33, the frequency acquisition loop is comprised of the phase and frequency detector (505), charge pump (535), oscillator (515) and divider (525) in Figure 5. Since this loop does not receive the binary signal (i.e. data 565) as an input to the phase and frequency detector (505), it does not appear that the loop maintains a relationship between the frequency of the binary signal and the frequency of the extracted clock signal, as recited in the claims. Since the extracted clock signal and the reference clock are provided as inputs to the phase and frequency detector (505), the frequency acquisition loop is maintaining a frequency relationship between these two input signals. Page 9, lines 25-31 also describes a frequency lock detector that determines the frequency difference between the extracted clock and ***the reference clock*** which appear to correspond to the limitations recited in claims 6 and 23.

Furthermore, although Figure 4 shows a clock and data recovery circuit 420 that maintains "a frequency between an extracted clock 430 and a binary signal D3" (see page 11 of the remarks), the drawings do not show the recited ***frequency acquisition loop*** for maintaining "a fixed relationship between a frequency of the binary signal and the frequency of the extracted clock signal." Therefore, the objections to the drawings and specification are not withdrawn.

As indicated by the Examiner in the Office Action of May 9, 2007, these objections may be overcome by amending "frequency of the binary signal" to "frequency of ***a reference signal***" in claims 5, 6, 18, 19, 22, 23, 25 and 26.

3. In response to applicant's argument that page 7, lines 24-30 describes how the equalization coefficient is modified (see page 13), the detailed description mentions adjusting the equalization coefficient but it does not disclose ***how*** the coefficient is modified to synchronize the frequencies (as recited in claim 25). Therefore, one of ordinary skill in the art is unable to make and/or use the invention and the rejection under 35 USC 112, 1st paragraph is not withdrawn.

4. In response to applicant's argument that Tomita does not generate an extracted clock signal from the equalized data as recited in claims 1 and 21 (see pages 14-15), Figures 1 and 3 of Tomita show generating a clock signal from a signal (e.g. RD) that has been filtered via feed forward filter 21 and/or feedback filter (25). Since the filtered

signal is "equalized," Tomita discloses generating an extracted clock signal from equalized data. Therefore, the rejection is not withdrawn.

5. In response to applicant's argument that the equalized data is not received by the clock and data recovery circuit as recited in claim 3 (see page 15), the admitted prior in Figure 3 of the present application discloses the claimed decision feedback equalizer whereas Tomita discloses the generation of a clock signal from the equalized/binary signal. The combination of the admitted prior art and Tomita discloses the claimed invention of claim 3. Therefore, the rejection is not withdrawn.

6. In response to applicant's argument that the admitted prior art is improperly applied to claims 5 and 22 (see page 15), the applicant admits that the clock and data recovery circuit in Figure 5 is "conventional" (see page 16, line 4). Therefore, assuming the frequency acquisition loop is maintaining a fixed frequency relationship between the extracted clock signal and ***a reference signal***, Figure 5 of the present application discloses the frequency acquisition loop and phase lock loop and the rejection is not withdrawn.

7. In response to applicant's argument that Kim does not disclose adjusting a frequency or phase of an extracted clock signal (see page 16), Figure 1 of Kim shows an extracted clock signal (INTCK) and Figures 2 and 3 show the adjustment of the

frequency and phase of INTCK. Therefore, the cited references in combination disclose the claimed invention and the rejection is not withdrawn.

Drawings

8. The drawings were received on July 27, 2007. These drawings are acceptable.

9. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the frequency acquisition loop that adjusts the frequency between the extracted clock signal and the binary signal (see claims 5, 6, 18, 19, 22, 23, 25 and 26) must be shown or the feature(s) canceled from the claim(s). In Figure 5, the loop that includes the phase and frequency detector 505 seems to adjusting the frequency between the extracted clock signal and a reference clock, not the binary signal (i.e. "Data"). (See also, page 8, lines 14-25) No new matter should be entered.

This objection may be overcome by amending "frequency of the binary signal" to "frequency of ***a reference signal***" in claims 5, 6, 18, 19, 22, 23, 25 and 26. (See the Claim Objections below)

10. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

11. Corresponding to the drawing objection above, the disclosure is objected to because the detailed description does not describe a frequency acquisition loop that maintains the frequency between the extracted clock signal and ***the binary signal*** (see claims 5, 6, 18, 19, 22, 23, 25 and 26. If the claims are amended to use the frequency acquisition loop to maintain the frequency between the extracted clock signal and ***a reference signal*** (see the Claim Objections below), this objection will be withdrawn. Appropriate correction/clarification is required.

Claim Objections

12. Claims 5, 6, 18, 19, 22, 23, 25 and 26 are objected to because of the following informalities:

a. in claim 5, line 5; claim 18, lines 4-5; claim 22, line 2; and claim 25, lines 2-3, "the binary signal" should be "***a reference*** signal"; and

b. in claim 6, line 4; claim 19, line 4; claim 23, line 4; and claim 26, line 3, "the binary signal" should be "the ***reference*** signal."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

13. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

14. Claims 7, 25, 26 and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

15. With regard to claim 7, the detailed description does not describe how the equalization coefficient changes during each iteration to synchronize the clock and data recovery circuit with the frequency of the equalized data. For example, does the value

of the equalization coefficient increase or decrease and under what conditions does it increase and/or decrease?

16. With regard to claims 25 and 26, the detailed description does not describe how the equalization coefficient is modified to synchronize the frequencies of the extracted clock signal and the binary signal, as recited in claim 25. Based on Figure 5, the synchronization does not seem related to or affected by the equalization coefficient. For example, does the value of the equalization coefficient increase or decrease and under what conditions does it increase and/or decrease?

17. Dependent claim 26 is rejected for the same reason as claim 25.

18. With regard to claim 28, the detailed description does not describe how the equalization coefficient is adjusted based on the frequency difference exceeding the threshold. For example, does the value of the equalization coefficient increase or decrease and how much does the coefficient value change?

19. Claims 8 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification, as originally filed, does not describe a multiplier that is configured to vary the equalization coefficient as recited in claim 8, lines 5-6 and claim 20, lines 2-3. Although specification, as originally filed, describes varying the value of the equalization coefficient, it does not describe the

multiplier as performing this function. The multiplier applies the variable equalization coefficient but it does not ***change*** or ***adjust*** it. Therefore, claims 8 and 20 do not comply with the written description requirement of 35 U.S.C. 112, first paragraph.

Claim Rejections - 35 USC § 103

20. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

21. Claims 1-5, 17, 18, 21, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in the present application in view of Tomita (US Patent No. 6,931,088 B1 cited in the Office Action mailed May 9, 2007).

22. With regard to claims 1-4 and 21, the admitted prior art in the present application discloses the claimed invention (see Figure 3; page 1, lines 23-33; and page 3, lines 7-27) except for generating the extracted clock signal from the equalized data.

Tomita discloses using an equalized signal to generate the clock for the retimer. (See Figures 1 and 3) It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Tomita and the admitted prior art in order to accurately synchronize the clock signal and recovered signal.

23. With regard to claim 17, the admitted prior art in the present application discloses the claimed invention (see Figures 2 and 3; page 1, lines 23-33; and page 3, lines 7-27) except the clock and data recovery circuit generating the extracted clock signal from the binary signal.

Figure 1 of Tomita discloses using a binary signal (S4) to generate a clock for the retimer. (See column 1, line 63 - column 2, line 10) It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Tomita and the admitted prior art in order to accurately synchronize the clock signal and binary signal.

24. With regard to claims 5, 18 and 22, assuming that the frequency acquisition loop maintains a relationship between the frequency of the extracted clock signal and a reference signal (i.e. the claims language is amended to be consistent with the detailed description of Figure 5), the admitted prior art in the present application in view of Tomita discloses the claimed invention. Figure 5 discloses a "conventional clock and data recovery circuit" (see page 7, lines 29-30) with a frequency acquisition loop and a phase acquisition loop.

25. With regard to claim 24, the admitted prior art in the present application in view of Tomita discloses the claimed invention since it is implicit/inherent that an equalization coefficient must be applied to the decision feedback equalizer upon startup.

26. Claims 5, 6, 18, 19, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Tomita as applied to claims 3 and 21, respectively, above, and further in view of Kim et al. (US Patent No. 6,670,853 B2 cited in the Office Action mailed May 9, 2007). These rejections apply to claims 5, 6, 22 and 23 as recited (i.e. assuming that the drawings and specification are amended to be consistent with the claims language).

27. With regard to claims 5, 18 and 22, the admitted prior art in view of Tomita discloses the claimed invention except for (a) a frequency acquisition loop for maintaining a relationship between the frequency of the extracted clock signal and the frequency of the binary signal; and (b) a phase acquisition loop for maintaining a relationship between the phase of the extracted clock signal and the phase of the binary signal.

Figure 1 of Kim et al. discloses a frequency acquisition loop (110) and a phase acquisition loop (130). (See also column 1, lines 20-26 and column 3, lines 46-67) It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. with that of the admitted prior art in view of Tomita in order to reduce jitter and locking time. (See Kim et al., column 3, lines 19-21)

28. With regard to claims 6, 19 and 23, the admitted prior art in view of Tomita and Kim et al. also discloses a lock detector. (See 120 in Figure 1 of Kim et al.)

29. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Tomita and Kim et al., as applied to claim 6 above, and further in view of Lin et al. (US Pub. No. 2004/0120422 A1) wherein the Examiner assumes that the multiplier is applying a variable equalizer coefficient. (See the rejection of claim 8 under 35 U.S.C. 112, first paragraph above) The references, as applied to claim 6, disclose the claimed invention including a decision feedback equalizer comprising a multiplier coupled to the retimer wherein the multiplier applies an equalization coefficient to generate the equalized feedback signal. (See Figures 2 and

3 of the present application) However, the references, as applied to claim 6, do not teach varying the equalization coefficient based on a level of inter-symbol interference in the received data.

Since Lin et al. teaches adjusting equalization coefficients to remove inter-symbol interference (see paragraph [0012]), it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the equalization coefficient in the circuit disclosed by the references, as applied to claim 6, based on the level of inter-symbol interference in order to improve the accuracy of data recovery.

30. Claims 20 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references, as applied to claims 19 and 1, respectively, above, and further in view of Welland et al. (US Patent No. 5,786,951). The references, as applied to claims 19 and 1, respectively, above, disclose the claimed invention including a decision feedback equalizer comprising a multiplier configured to scale the recovered equalized signal. (See 270 and 300 in Figures 2 and 3, respectively, of the present application) However, the references do not teach an equalization coefficient based on a bit error rate of the received data.

Welland et al. discloses adjusting tap coefficients based on performance data to meet bit error rate criteria. (See column 4, lines 16-24) It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the equalization coefficient in the circuit disclosed by the references, as applied to claims 19

and 1, respectively, above, based on performance data such as bit error rate in order to improve the accuracy/reliability of the recovered data.

Terminal Disclaimer

31. The terminal disclaimer filed on July 27, 2007 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the full statutory term of any patent granted on pending Application Number 10/774,725 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Conclusion

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Betsy L. Deppe whose telephone number is (571) 272-3054. The examiner can normally be reached on Monday, Wednesday and Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

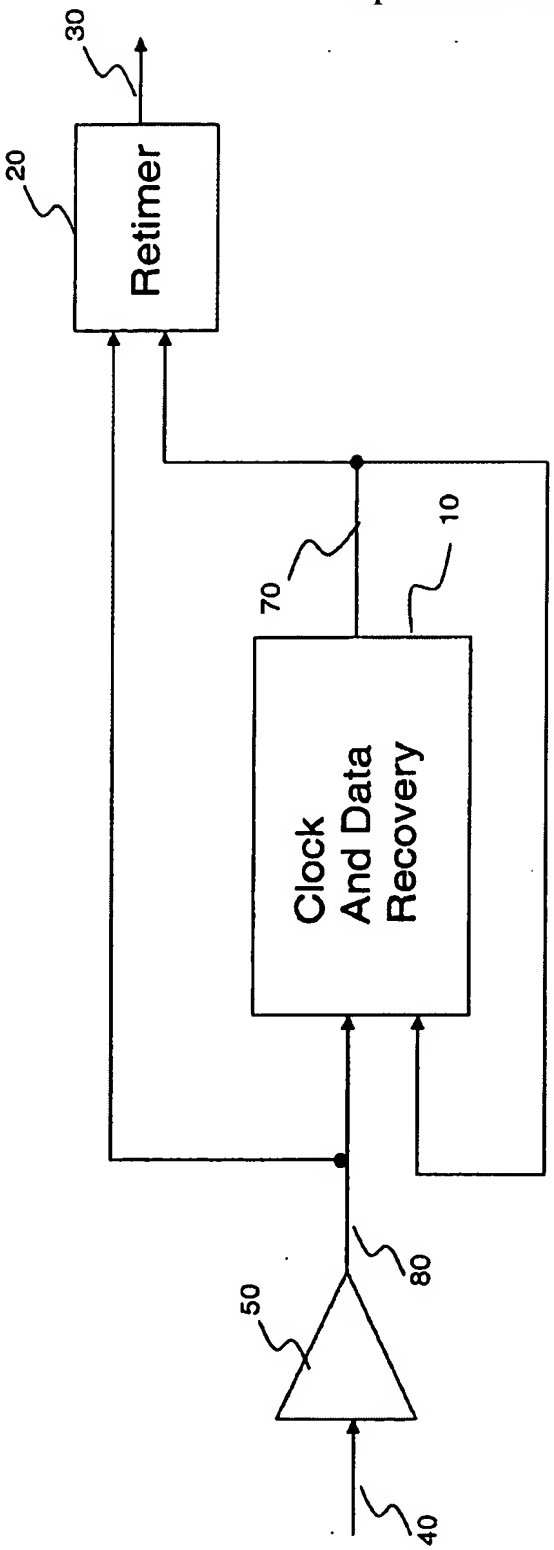
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Betsy L. Deppe
Primary Examiner
Art Unit 2611

Replacement Sheet

Replacement sheets. Acceptable
BD 9/10/07



Prior Art

FIG. 1